Amendments to the Drawings:

The attached sheets of drawings include changes to Fig. 1A, 1B, 2B and 9B. These sheets, which include Fig. 1A, 1B, 2B, 9A and 9B, replace the original sheets.

Attachments: Replacement Sheets (04)
Annotated Sheets Showing Changes (04)

REMARKS/ARGUMENTS

The Examiner is thanked for her thorough examination and helpful comments in the Office Action. The undersigned also thanks the Examiner for granting an in-person interview to the Applicant on November 17, 2004. As was proposed during the interview, solely in order to expedite prosecution, the Applicant has amended claim 1 to further recite the features of claim 9. In addition, claim 1 has been further clarified. As noted during the interview, claim 9 is supported, for example, by paragraphs 27-30 (see Figs. 2A and 2B), and paragraphs 38-41 (Figs. 6A and 6B).

It should also be noted that more details about the Java Bytecode translator 230 and inventive Java instructions 1-N (shown in Fig. 2b) are described in U.S. Patent Application No. 09/819,120, entitled "REDUCED INSTRUCTION SET FOR JAVA VIRTUAL MACHINES," and U.S. Patent Application No. 09/820,097, entitled "ENHANCED VIRTUAL MACHINE INSTRUCTIONS." (See, specification, paragraph 29 on page 10). In addition, Appendix A also illustrates a mapping of conventional bytecodes to the reduced set of instructions in accordance with one embodiment of the invention.

As was discussed during the interview, it is respectfully submitted that the cited art does NOT or teach or suggest the combination of several features recited in claim 9. These features include: (a) selecting, at load time, a first-reduced instruction from a reduced set of virtual machine instructions such that the first-reduced instruction represents two or more different virtual machine instructions in a first sequences, (b) translating, at load time, two or more different virtual machine instructions in the first sequence into a first-reduced instruction from the reduced set of virtual machine instructions, (c) generating, after said translating, a second sequence of bytecodes that includes the first-reduced instruction, (d) determining, at load time, whether the second sequence of bytcodes includes an instantiation instruction immediately followed by a duplicate stack instruction, and (e) generating, at load time, a macro instruction that represents the instantiation instruction and duplicate stack instruction.

Proposed drawings of Fig. 1A, 1B, 2B and 9B with the corrections requested by the Examiner are hereby submitted herein.

It is respectfully requested that claims 2 and 9-21 be cancelled without disclaimer or prejudice. However, the Applicant reserves the right to pursue claims of original scope in a continuation application. New claims 22-35 recite similar features as those recited in claim 9 and its dependent claims. Accordingly, it is respectfully that all pending claims are in condition for early allowance.

Additional limitations recited in the independent claims or the dependent claims are not further discussed because the limitations discussed above are sufficient to distinguish the claimed invention from the cited art. Accordingly, Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner.

Applicants hereby petition for an extension of time which may be required to maintain the pendency of this case, and any required fee for such extension or any further fee required in connection with the filing of this Amendment is to be charged to Deposit Account No. 500388 (Order No. SUN1P839). Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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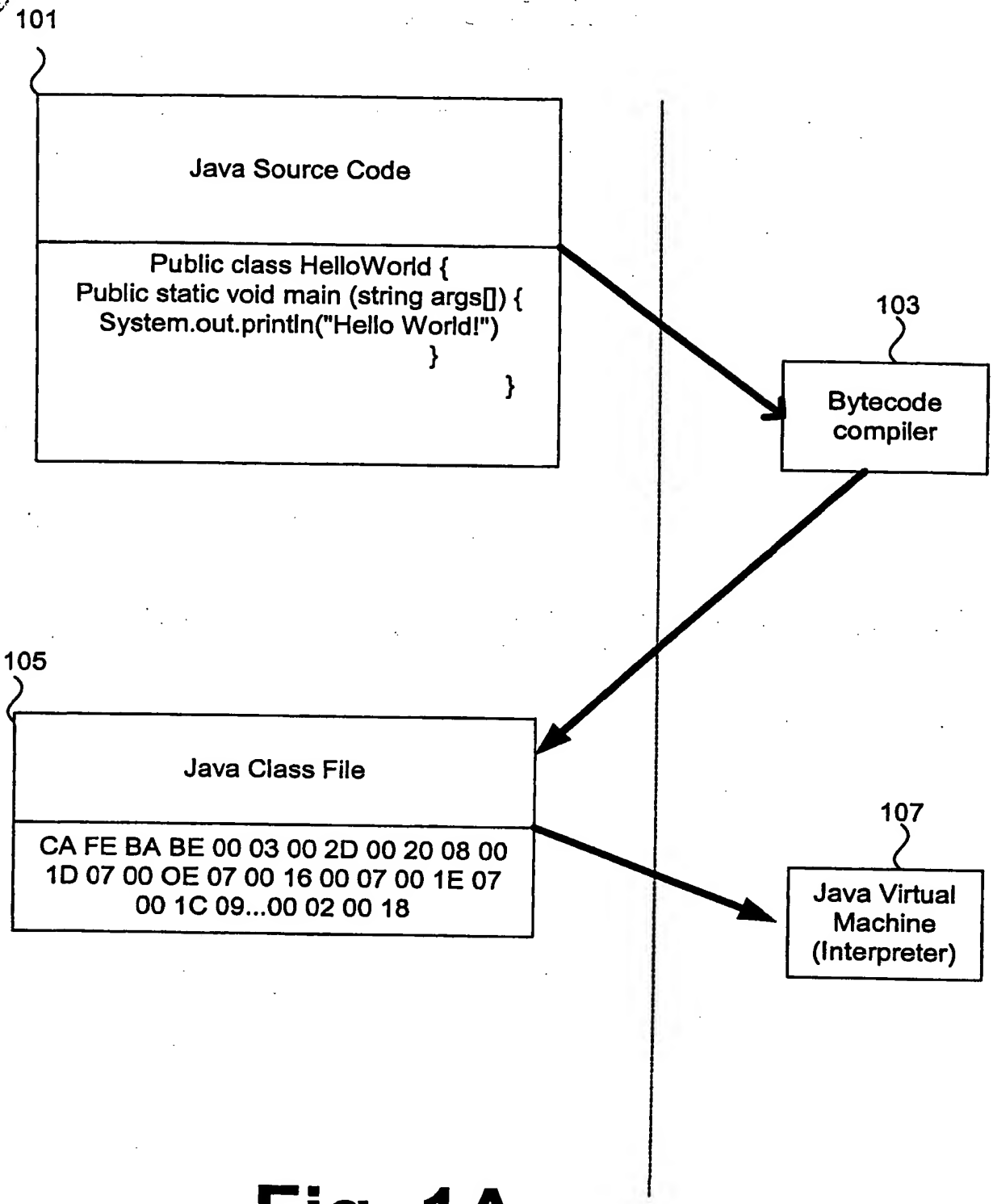

Fig. 1A

Prior Art

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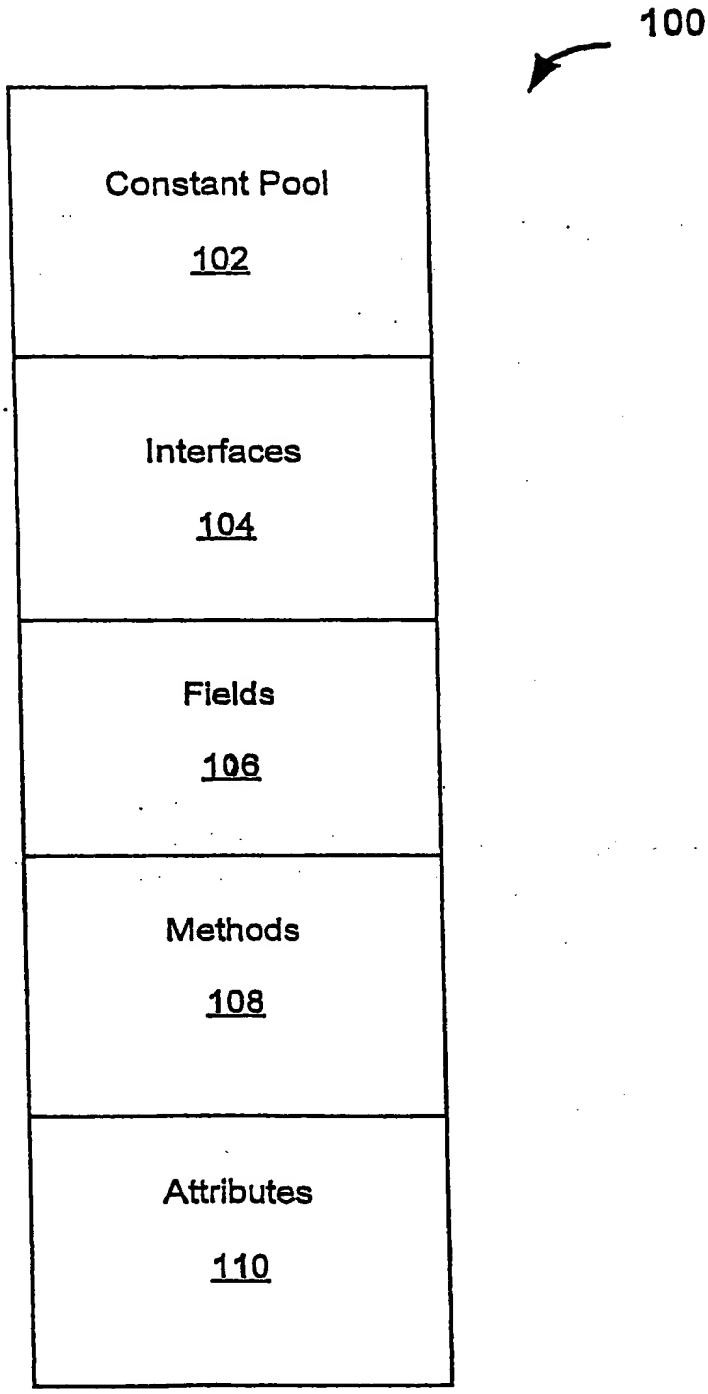

Fig. 1B

Prior Art

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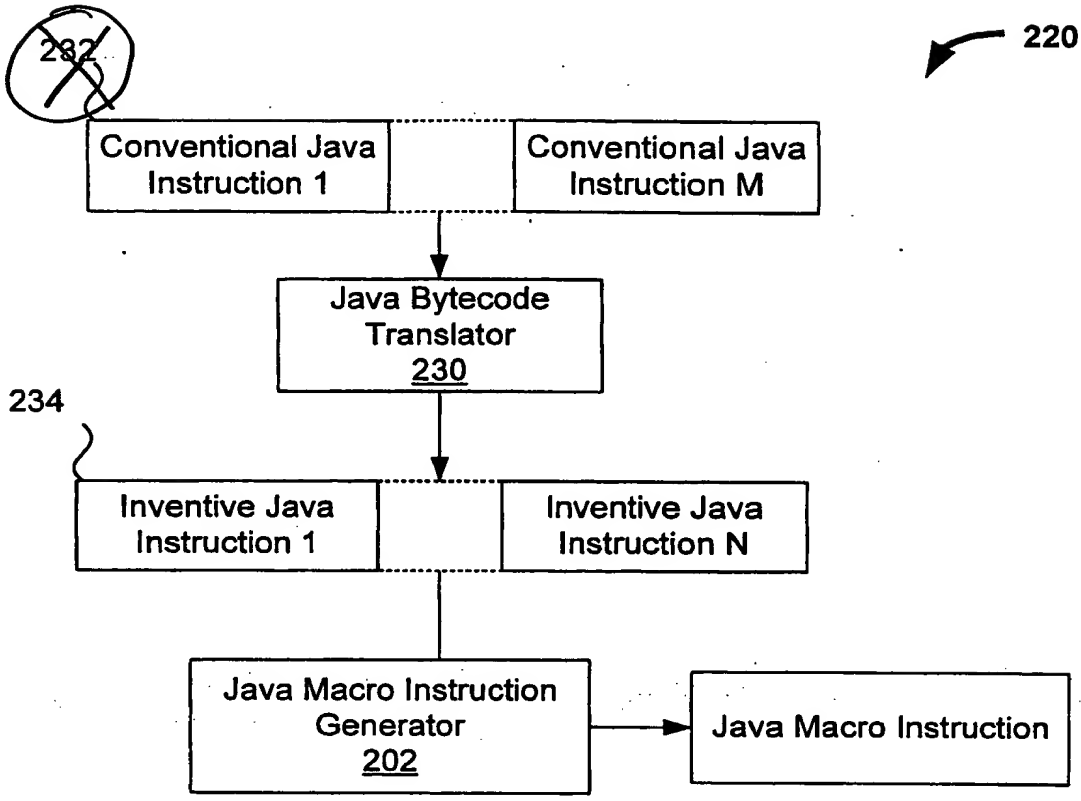

Fig. 2B

I.P.E.
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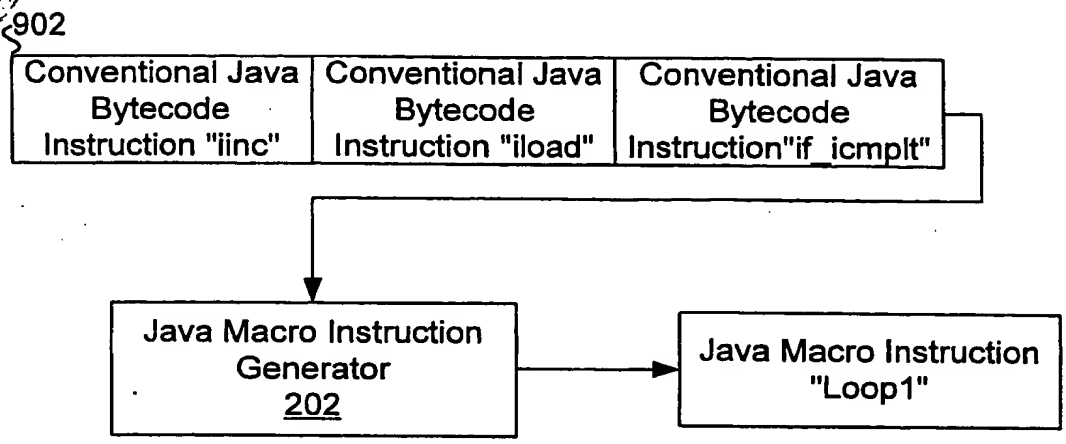

Fig. 9A

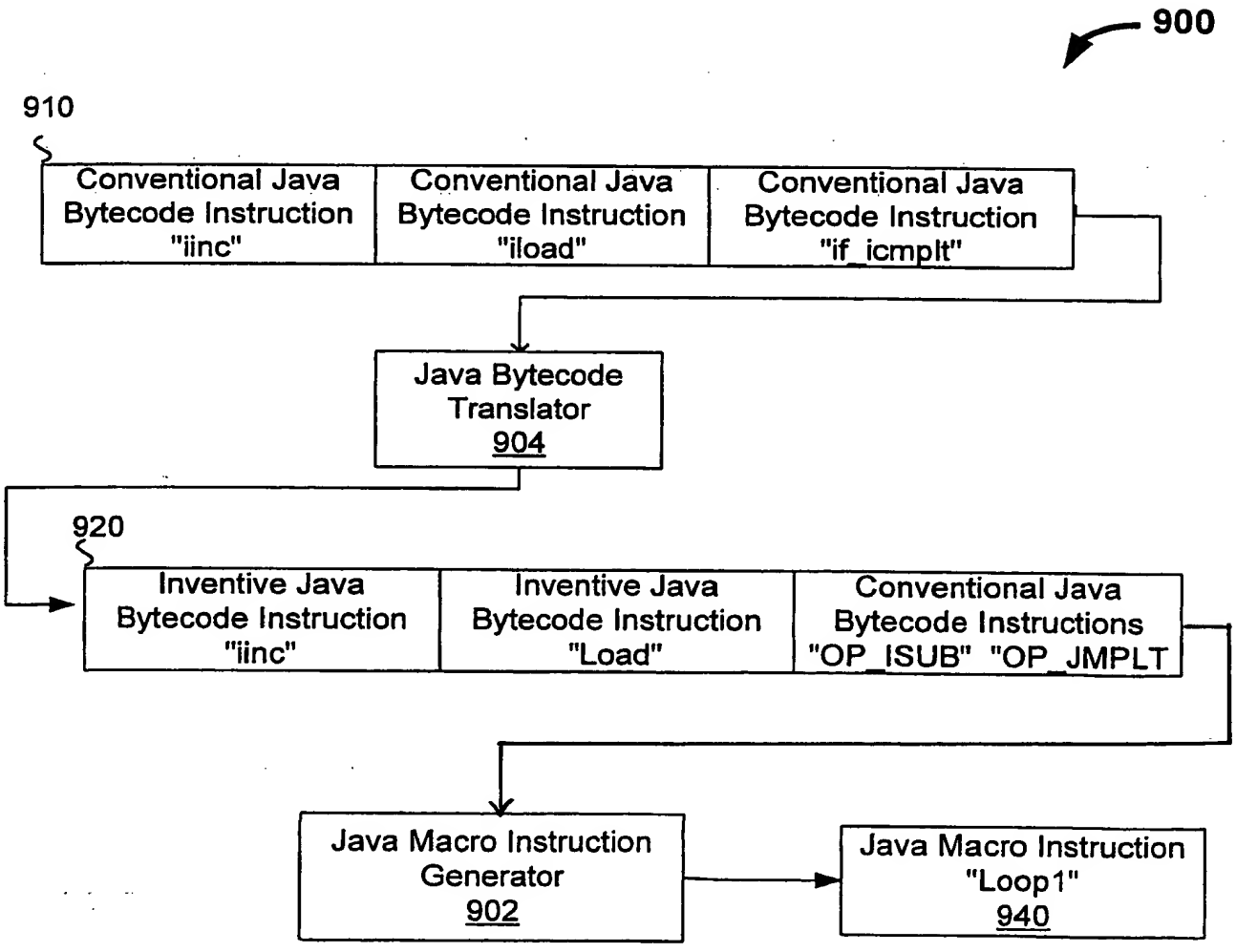

Fig. 9B